



H61H2-M2

Rev : 1.0

ECS CONFIDENTIAL

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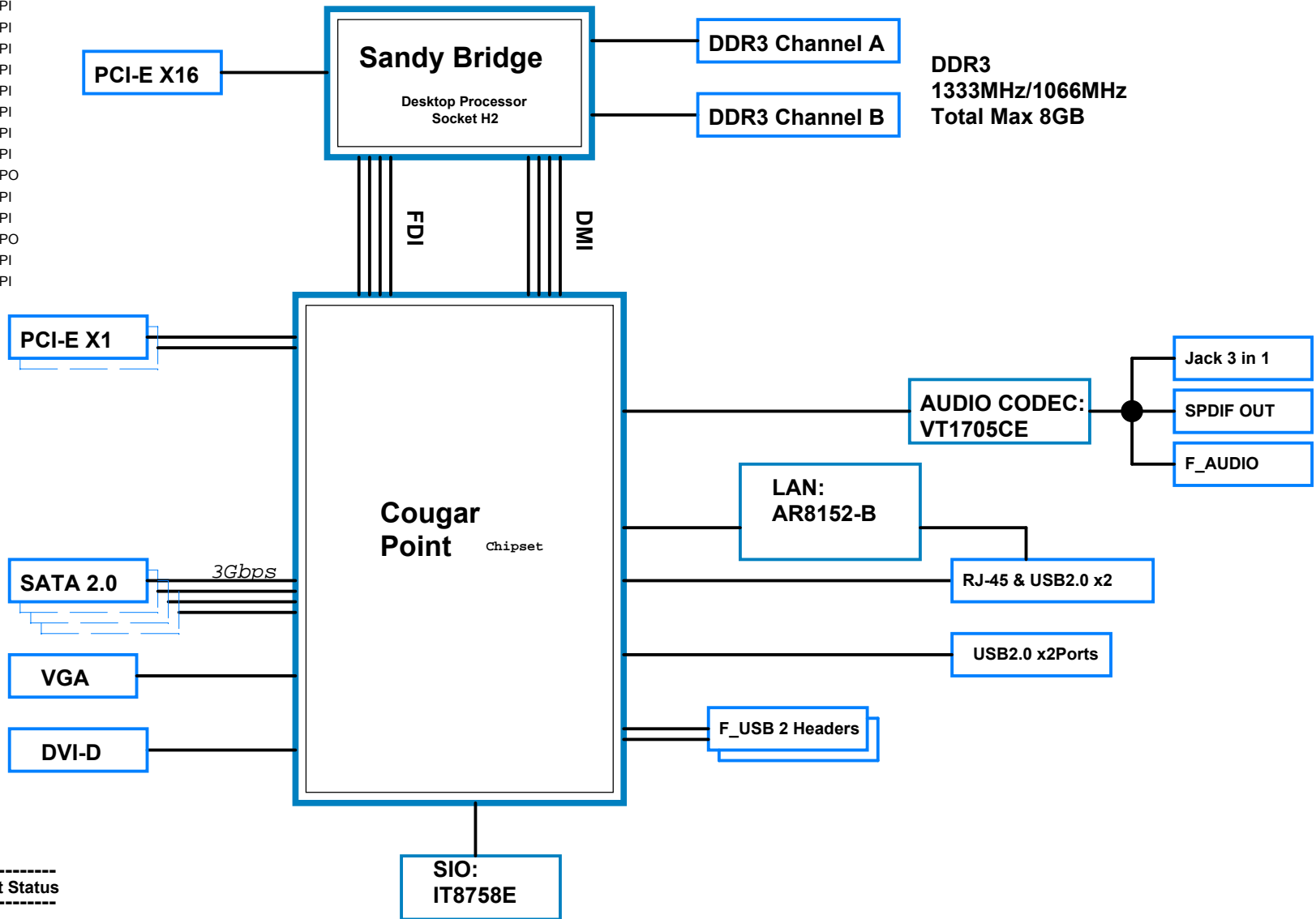
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REVISION HISTORY:

Rev	Date	Notes
V.A	2010/09/23	Change from H67H2-M3 1. Audio change to vt1705 2. Super IO change to IT8758E 3. VCore PWM change to RT8859M 4. V_CPUVTT PWM change to RT8121 5. LAN change to AR8151-B & AR8152-B 6. Del PCI function 7. Del USB3.0 function 8. Del SATA 6G 9.Del Easy Charge Circuit of F_USB1
V.1.0	2010/12/03	1. PSON- Pull High 從5VSB改為3VSB_IO 2. Del EC33 1000U-6.3DL-O 3. Change EC35 from (1000U-6.3DL) to (820U-2.5D6-OS) 4. Del EC24 100U-16DE-O 5. 更改DDR3 SOCKET 顏色為兩根都灰色 6. 更改BATTERY SOCKET換成非架高料 7. 更改POWER CONN. 24pin 換成半透明STD料 8. 更改F_USB1改成和F_USB2為相同的顏色 9.VT1705更改為VT1705CE 10.SATA0GP、SATA1GP、SATA2GP、SATA3GP、SATA4GP、SATA5GP 增加Pull High & Low線路

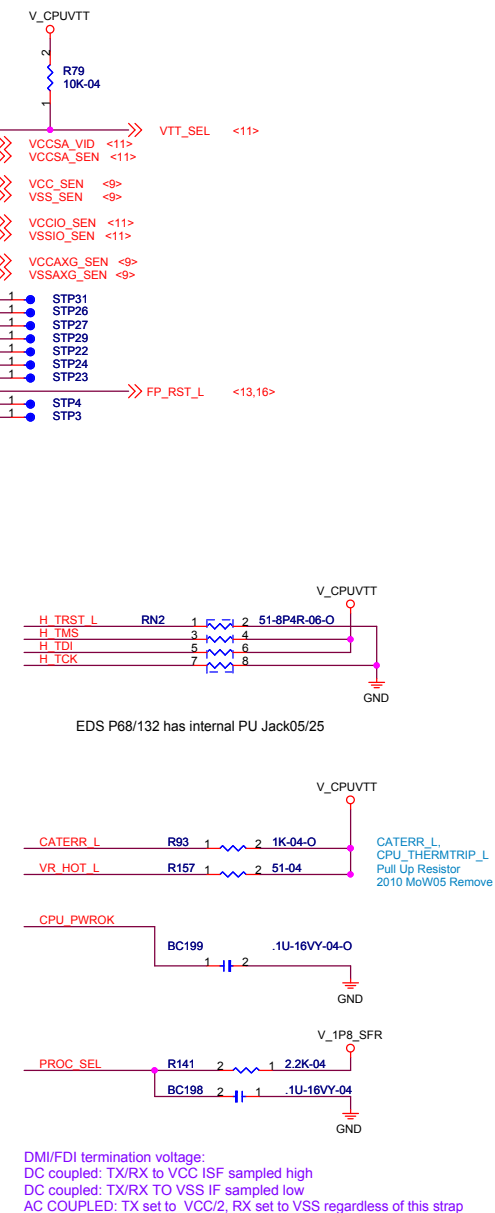
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI



SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	



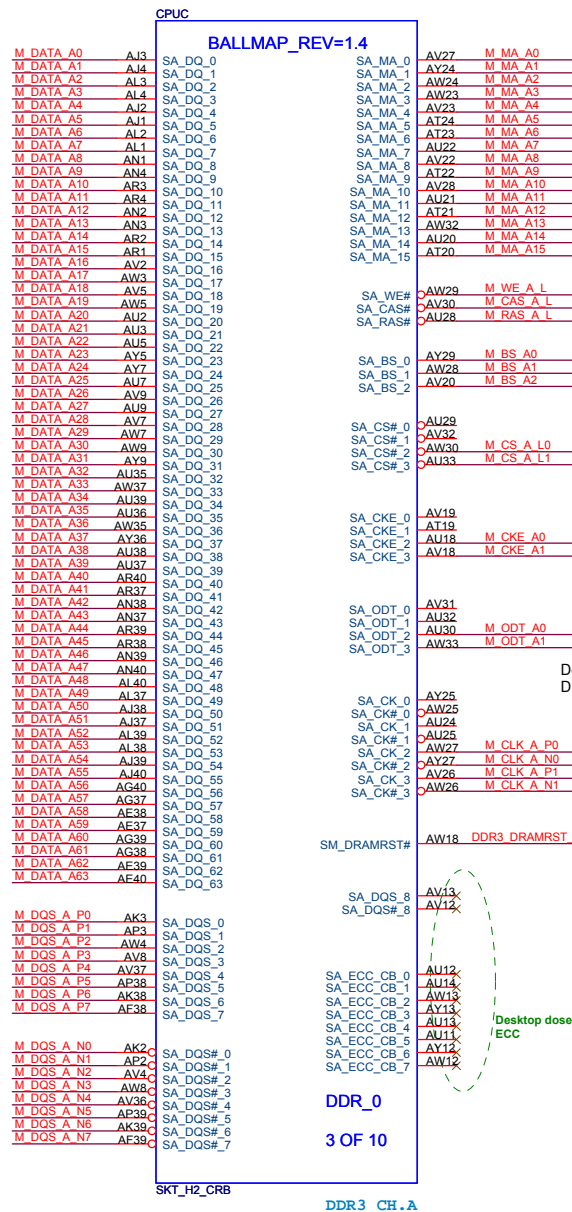
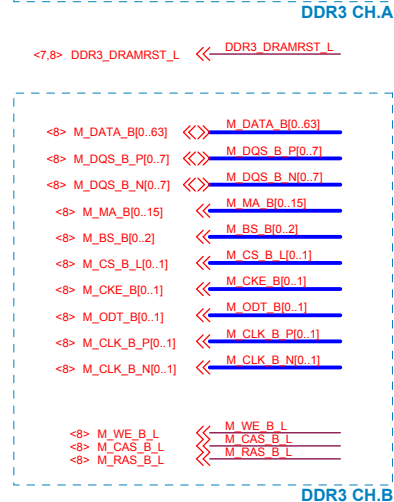
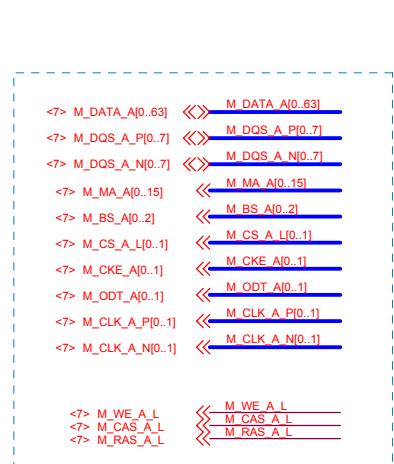
TO VRD FOR S0->S5

VR_EN

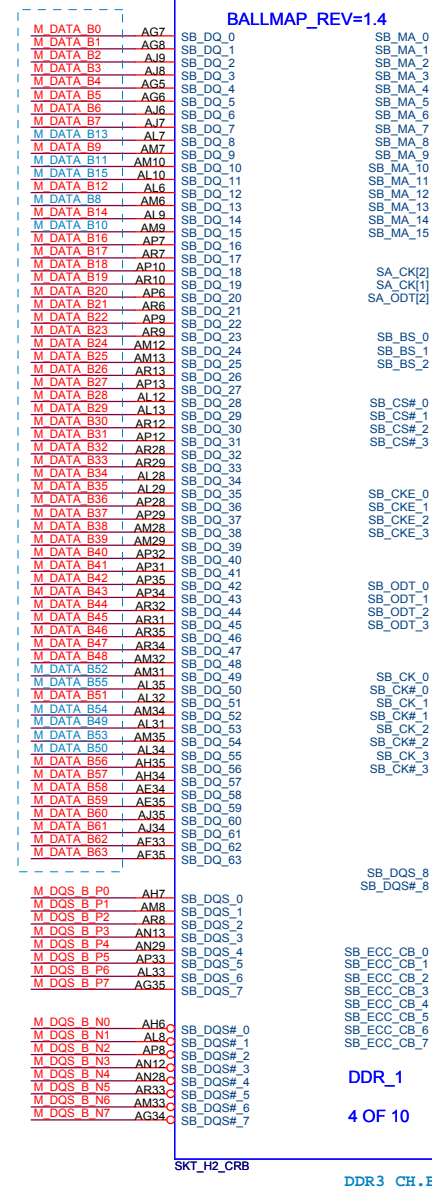
FROM VRD

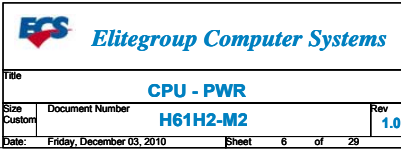
CPU_PWROK

20100927
Del By Andy lu

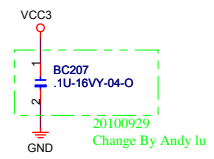
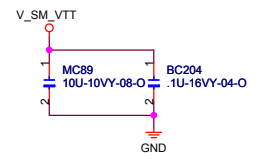
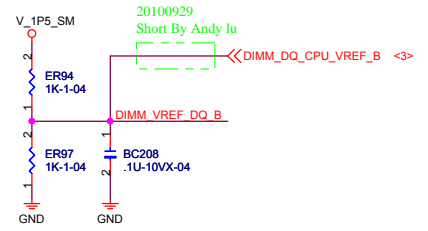
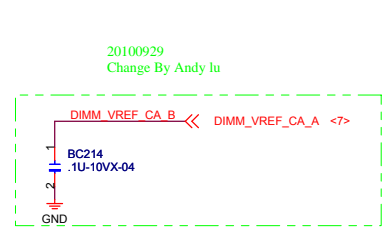
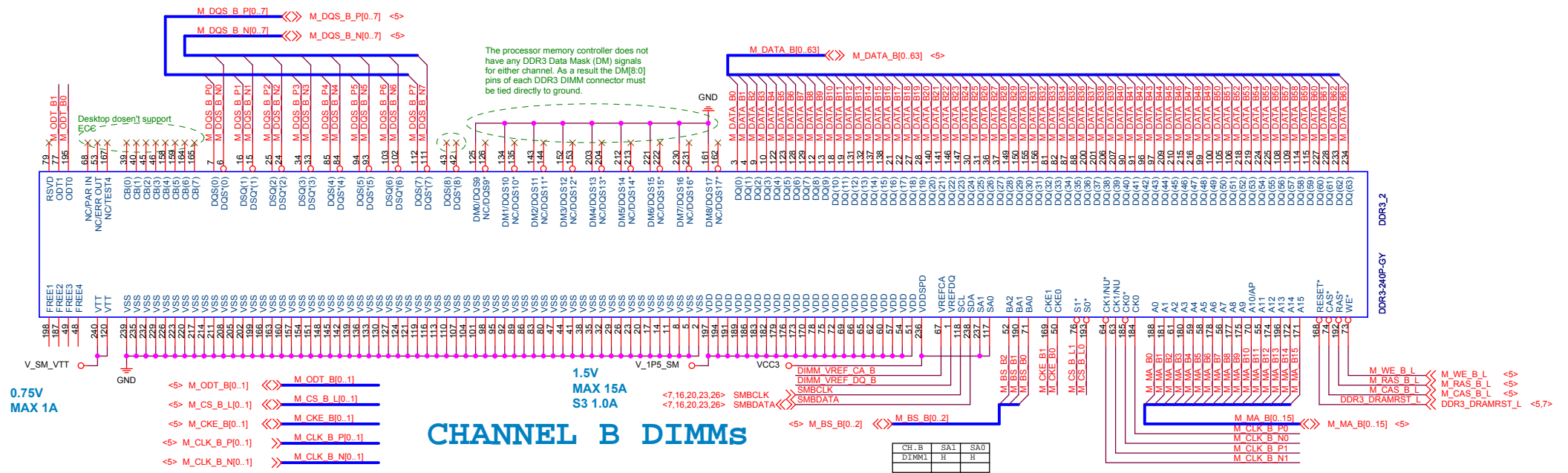


Pay Attention to This Part!





The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.



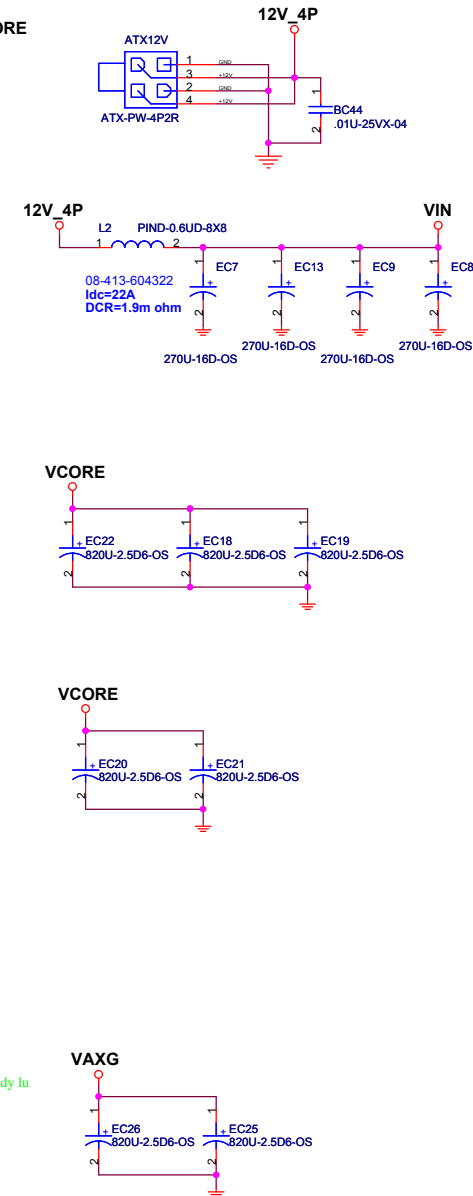
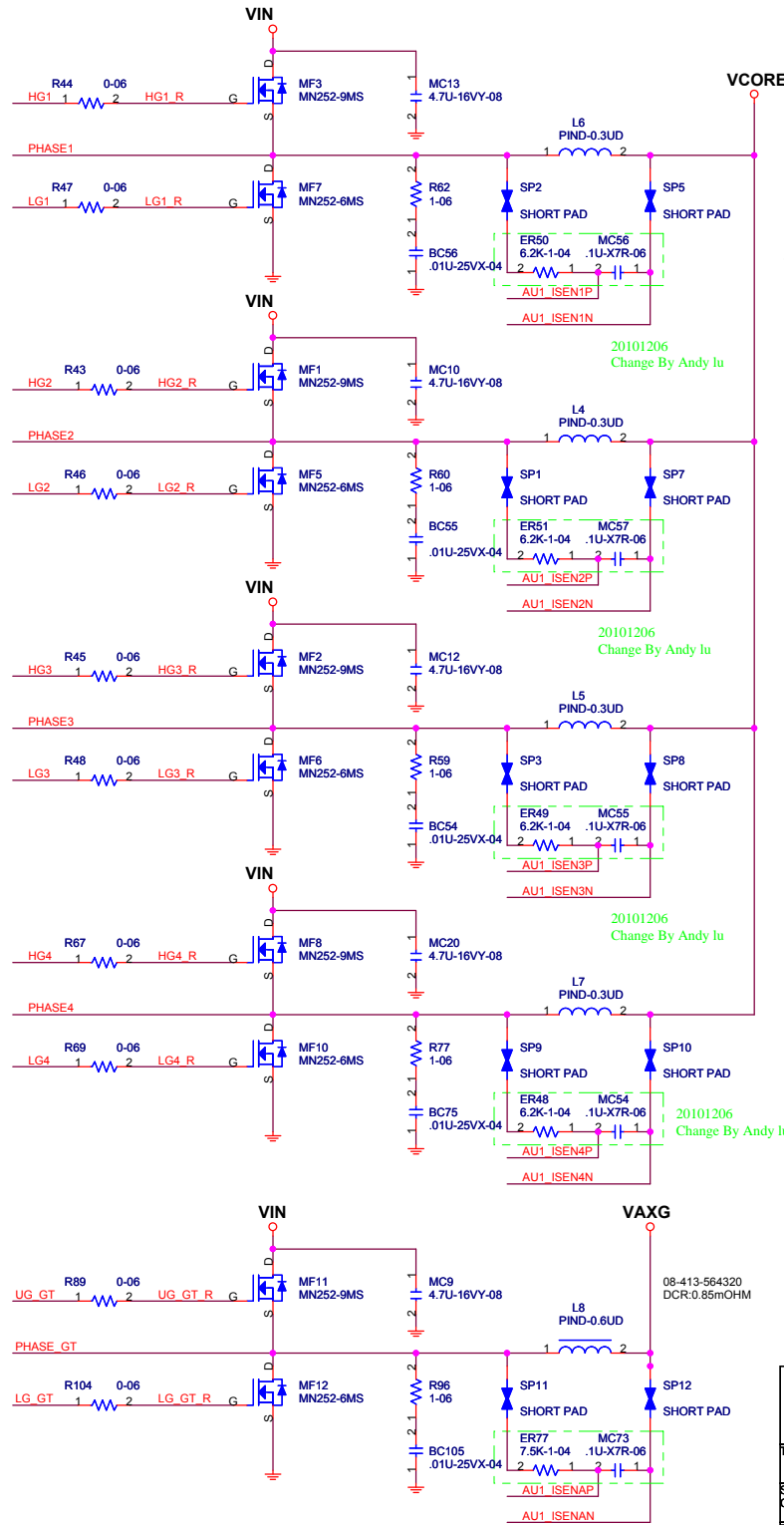
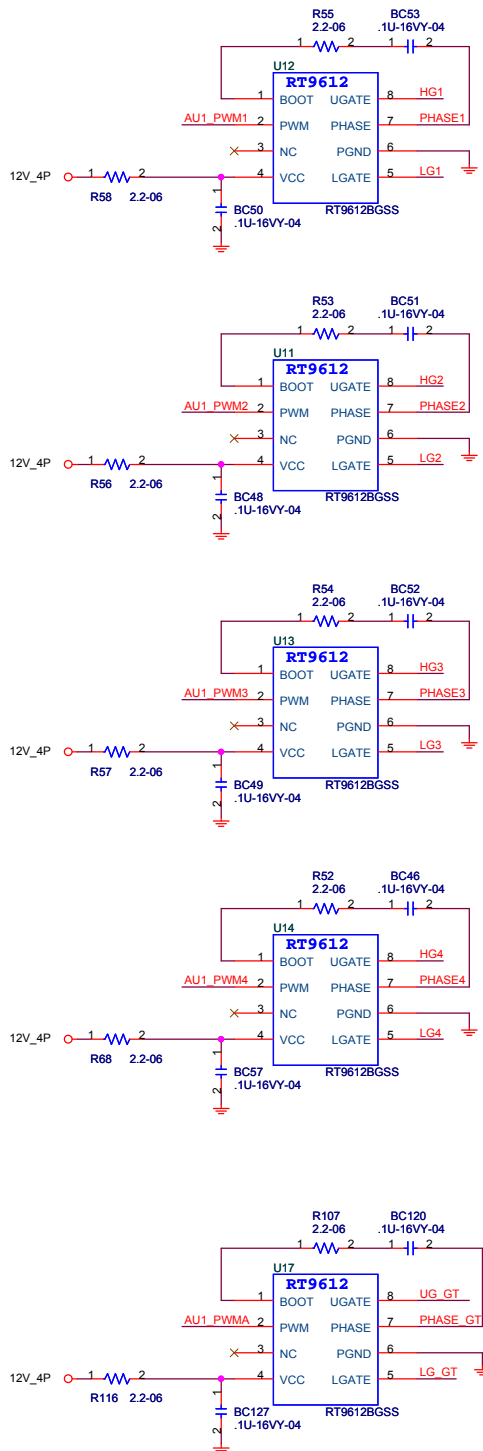
Del DIMM3 for always populate DIMM4 first Jack 05/13

External Connection

VCC ○ VCC
VCORE ○ VCORE
12V_4P ○ 12V_4P
VCC3 ○ VCC3
VIN ○ VIN
VAXG ○ VAXG

<9> AU1_PWM[1..4] ○ AU1_PWM[1..4]
<9> AU1_ISEN1P ○ AU1_ISEN1P
<9> AU1_ISEN1N ○ AU1_ISEN1N
<9> AU1_ISEN2P ○ AU1_ISEN2P
<9> AU1_ISEN2N ○ AU1_ISEN2N
<9> AU1_ISEN3P ○ AU1_ISEN3P
<9> AU1_ISEN3N ○ AU1_ISEN3N
<9> AU1_ISEN4P ○ AU1_ISEN4P
<9> AU1_ISEN4N ○ AU1_ISEN4N

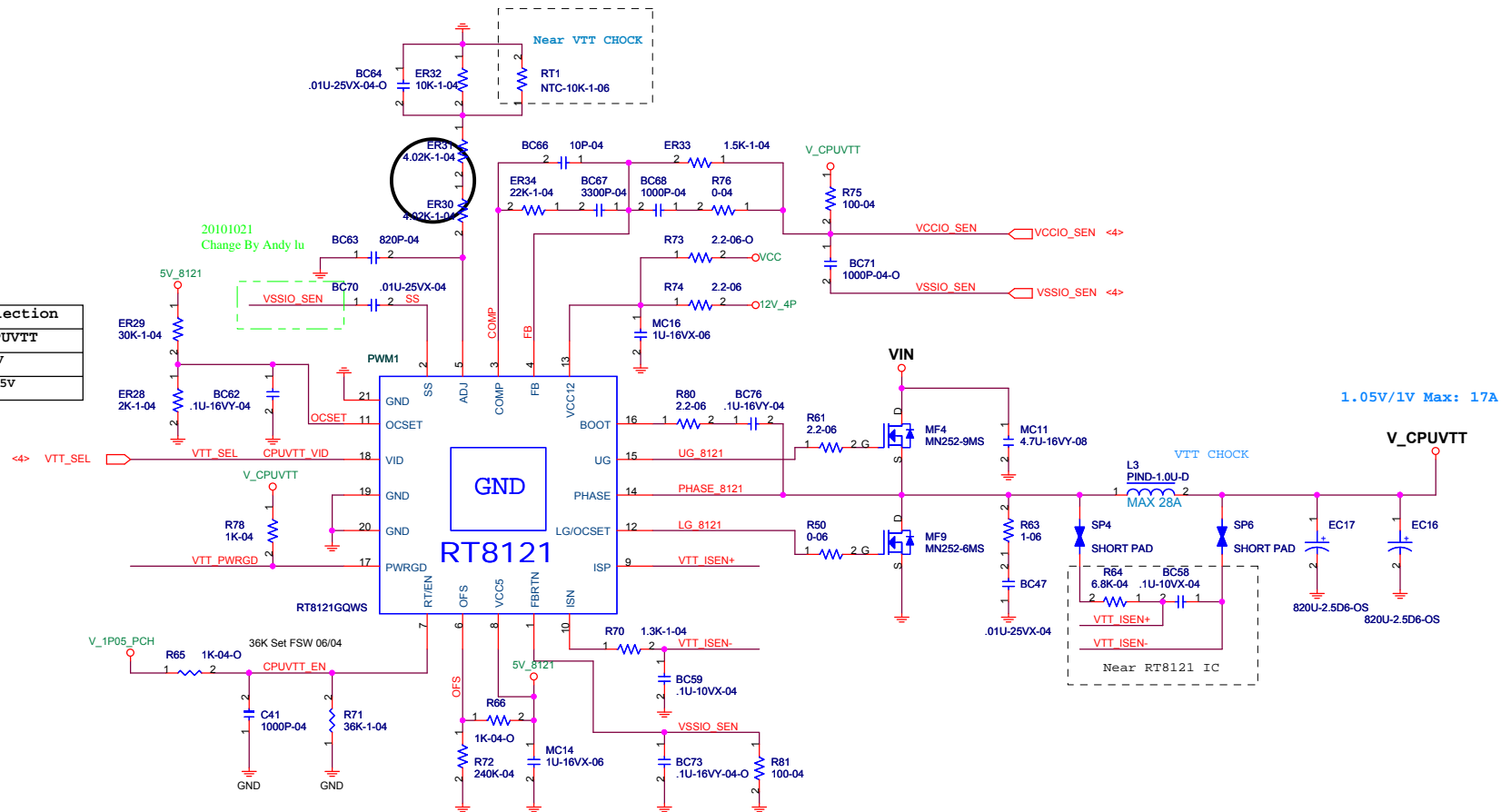
<9> AU1_PWMA ○ AU1_PWMA
<9> AU1_ISENAP ○ AU1_ISENAP
<9> AU1_ISENAN ○ AU1_ISENAN



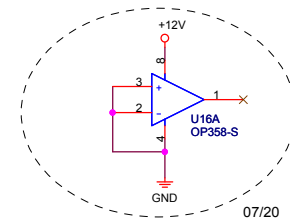
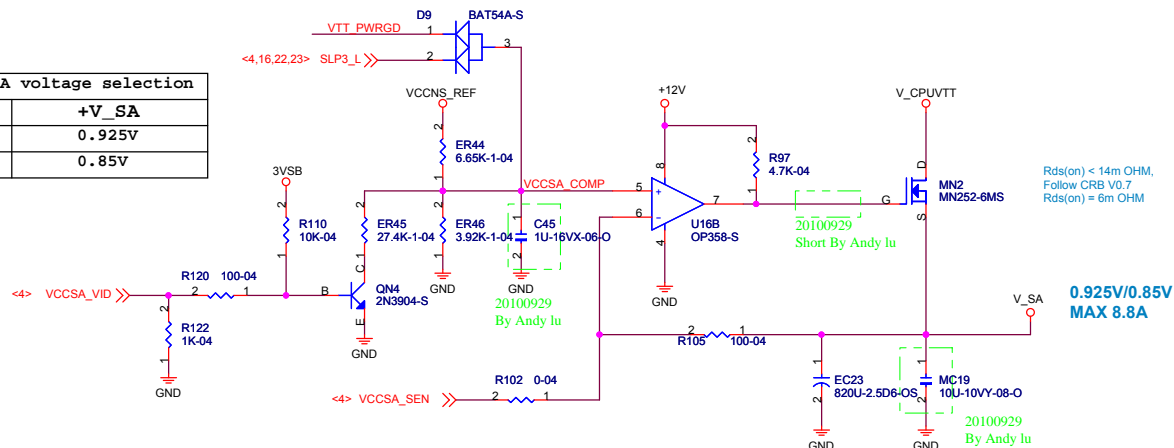
DC/DC VCORE/VAXG RT9612			
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Diagram showing the connection of the 5V pin to VCC, 3VSB, 5VSB, _1P05_PCH, and V_CPUVTT.

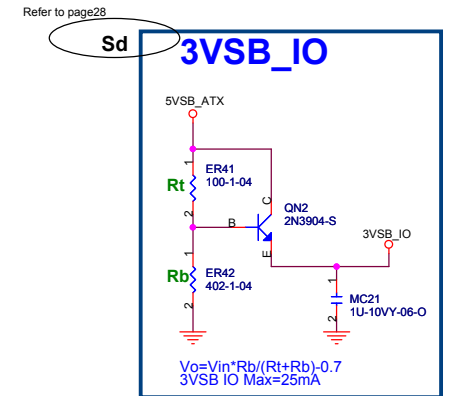
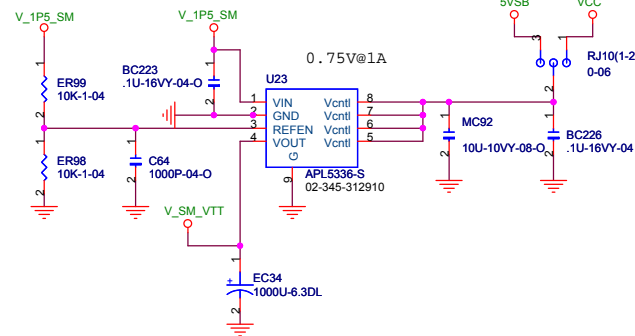
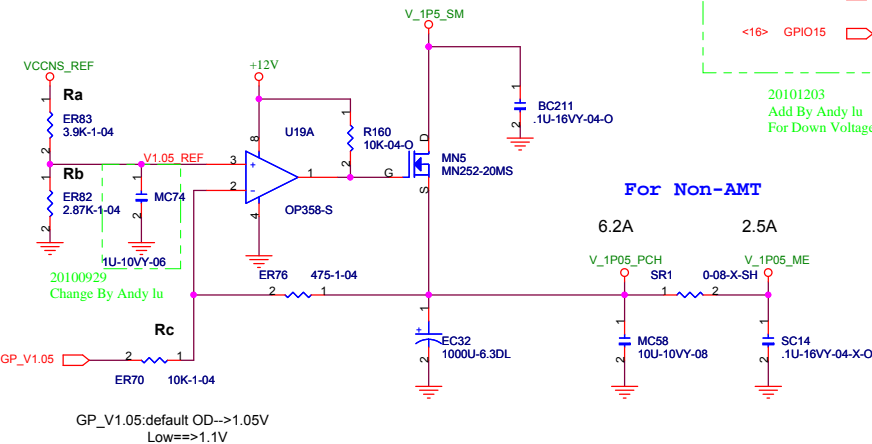
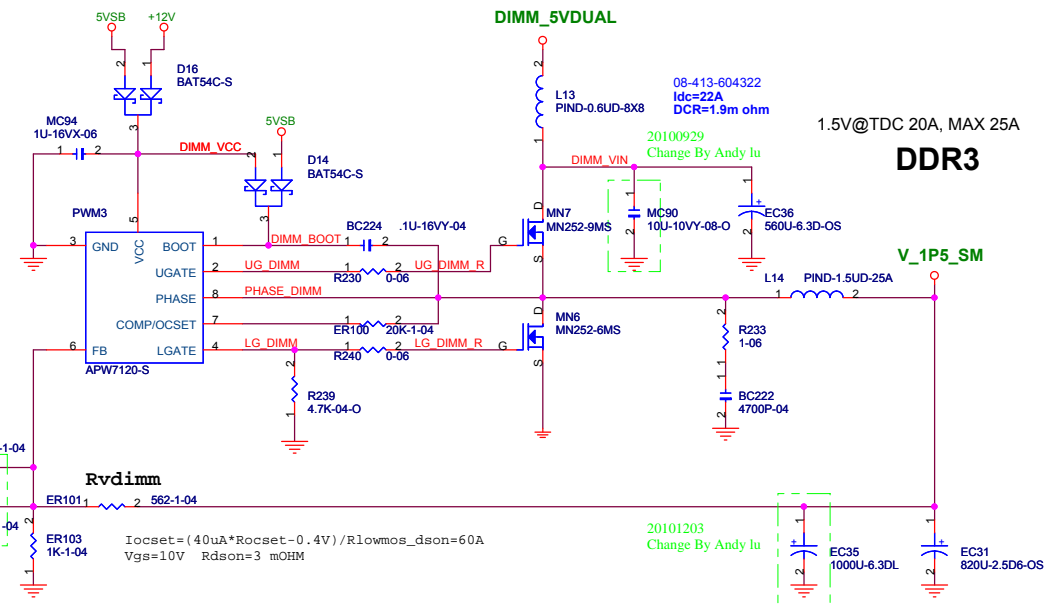
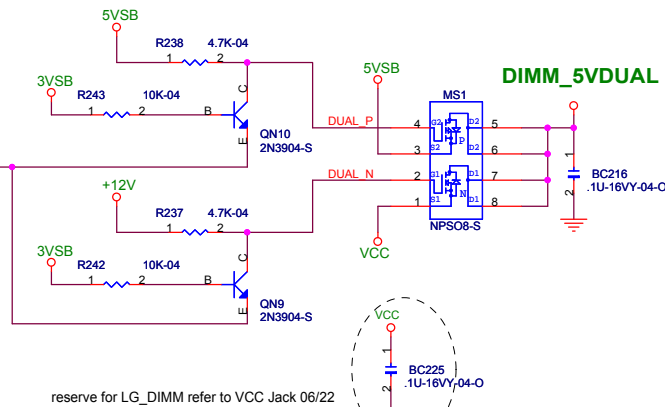
VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V



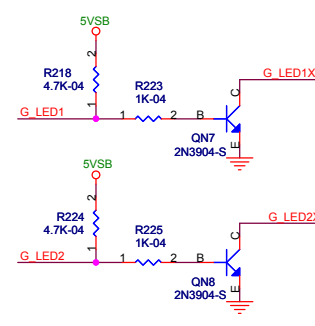
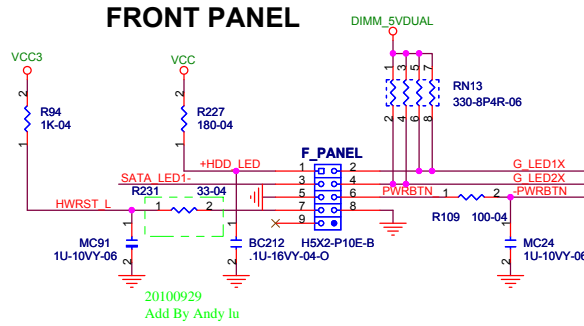
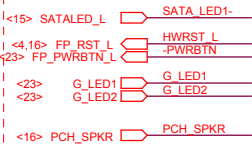
VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V



20100924
Change By Andy lu
From 3VSB to 5VSB

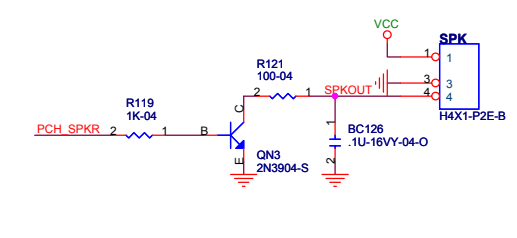


External Connection



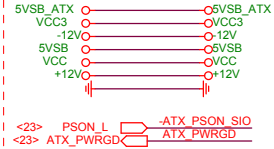
	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
G	GB	YB	IOFF	OFF	OFF

B: Blinking



POWER CONNECTOR

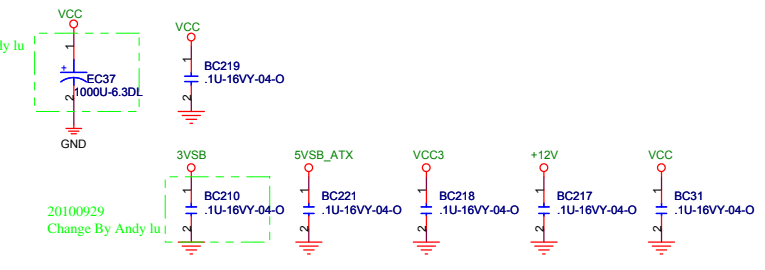
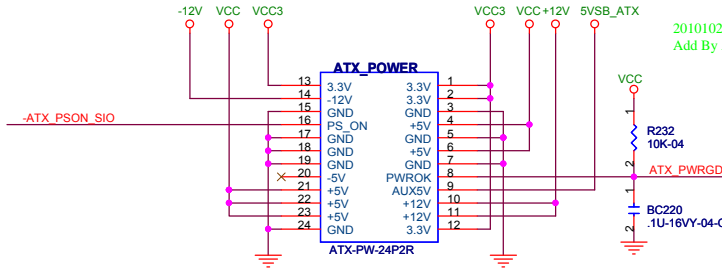
External Connection



F_PANEL

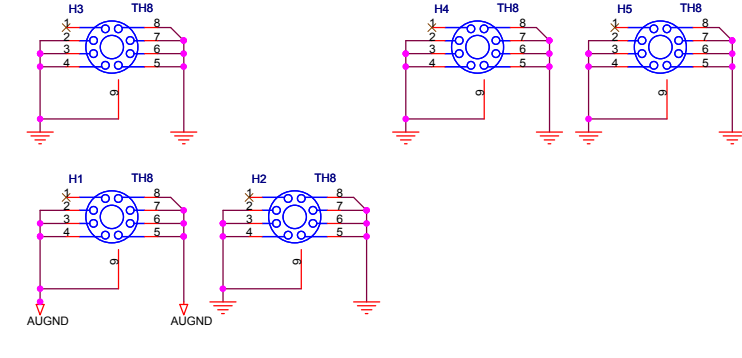
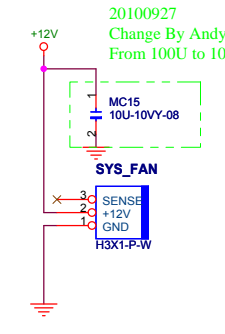
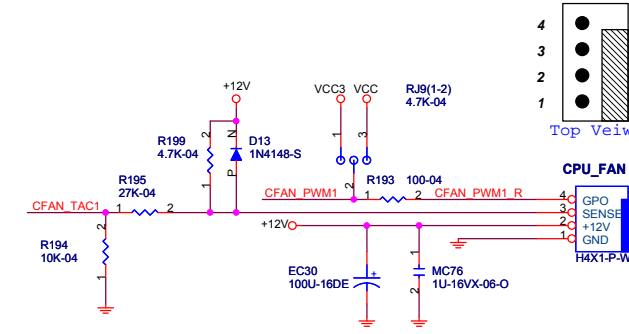
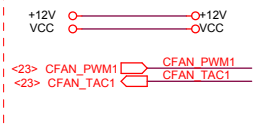
1	2
3	4
5	6
7	8
9	X

++HDDLED RST PWR

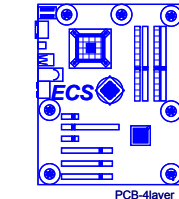


FAN

External Connection

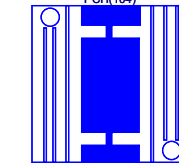


PCB



PCB-4layer

PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM



20-120-011476

5series PN:20-120-010851

CLR_CMOS(1-2)



JP-R

BT(104)



CR2032

Y1(wire)



JP-WI-P6.25

SMD 6.4M

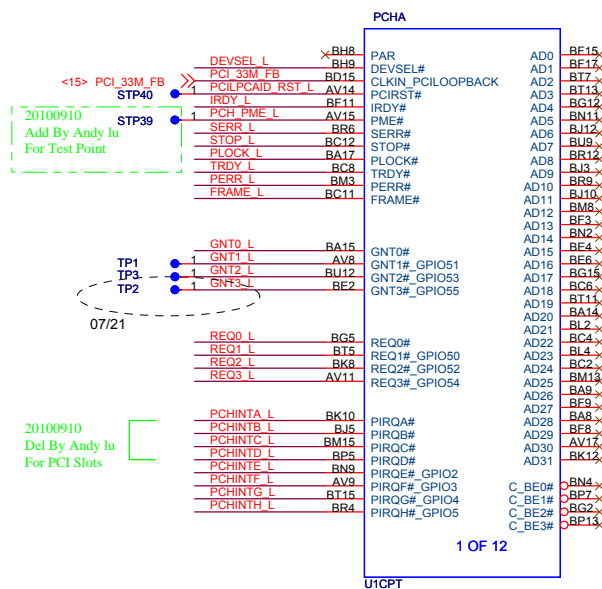
Elitegroup Computer Systems

Title: **Front Panel,FAN,PowerConn,GND,104**

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For H61:USB Port 6/7/12/13 is disabled....From 440377 file



20100910
 Del By Andy lu
 For PCI Slots

PCIEx1_A

<20> PEX1A_RX_N1
 <20> PEX1A_RX_P1
 <20> PEX1A_TX_N1
 <20> PEX1A_TX_P1

PCI bridge

20100910
 Del By Andy lu
 For PCI Bridge

20100909
 Add By Andy lu

PCIEx1_B

LAN

<26> LAN_RX_N6
 <26> LAN_RX_P6
 <26> LAN_TX_N6
 <26> LAN_TX_P6

For H61:PCIE 7/8 is disable....From intel Jasmine

GPIO19:
 Boot Device Select Strap.

GNT0_L:
 No More Information in EDS V0.7

GNT1_L:
 Boot Device Select Strap.

GNT2_L:
 ESI Strap (Server Only),
 DONT Pull Low in Desktop.

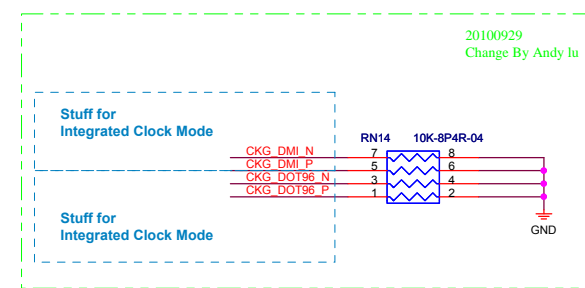
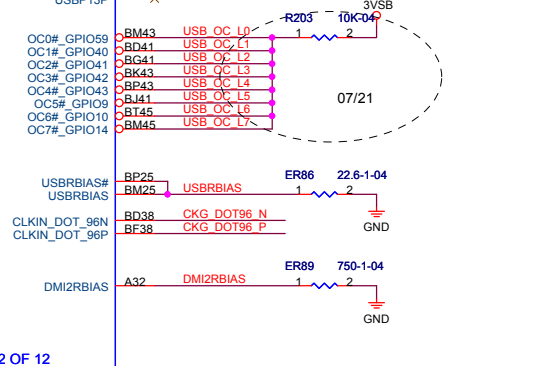
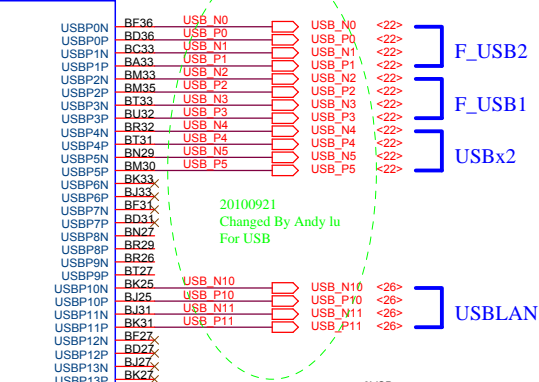
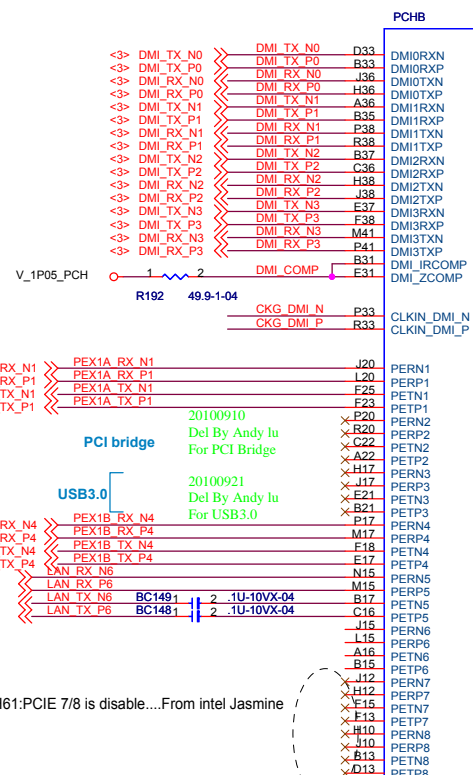
GNT3_L:
 Top-Block Swap Override Mode,
 When Sampled Low.

GNT[0..3]#
 GPIO19
 have been internal pull high to +VCC3

Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

*

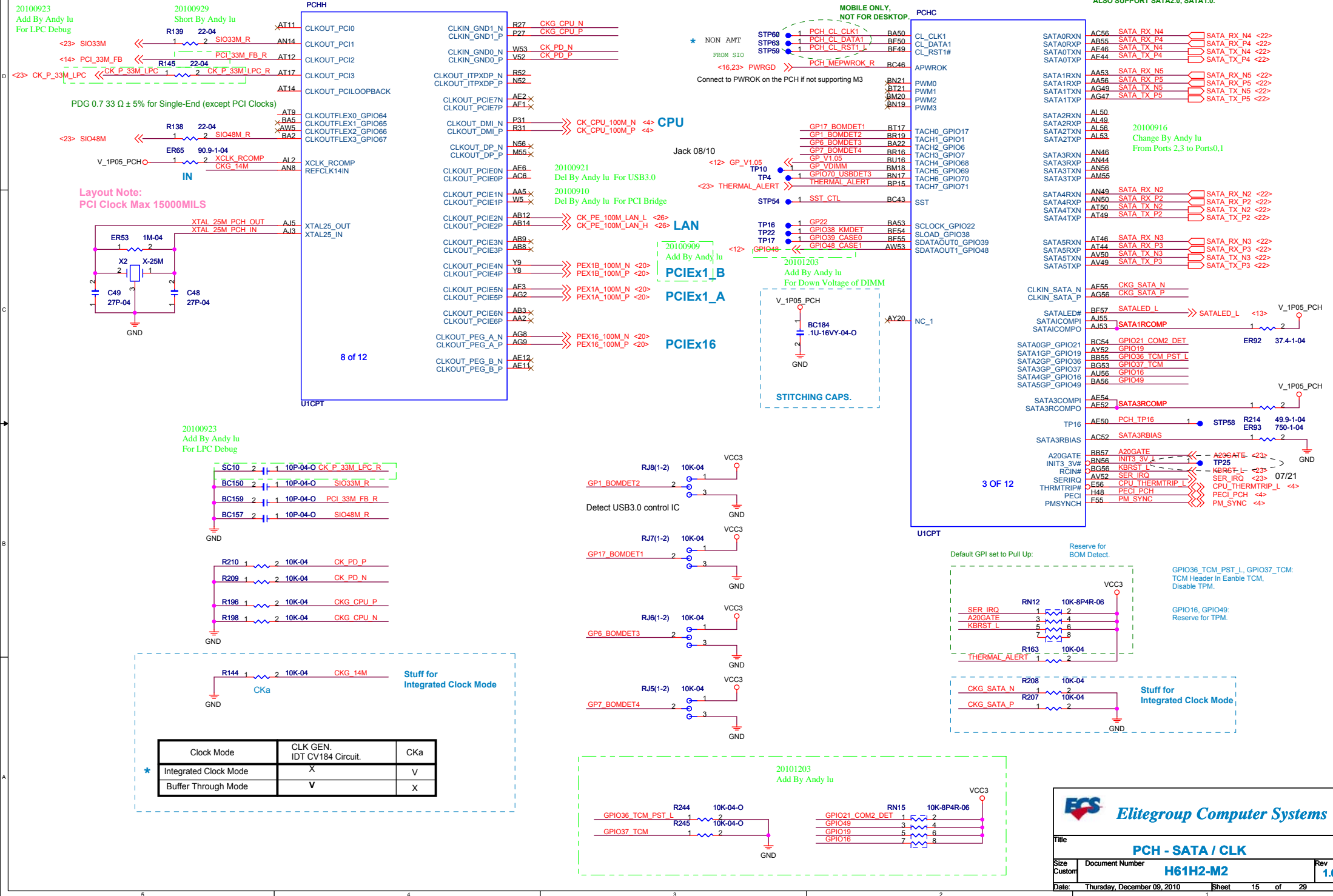


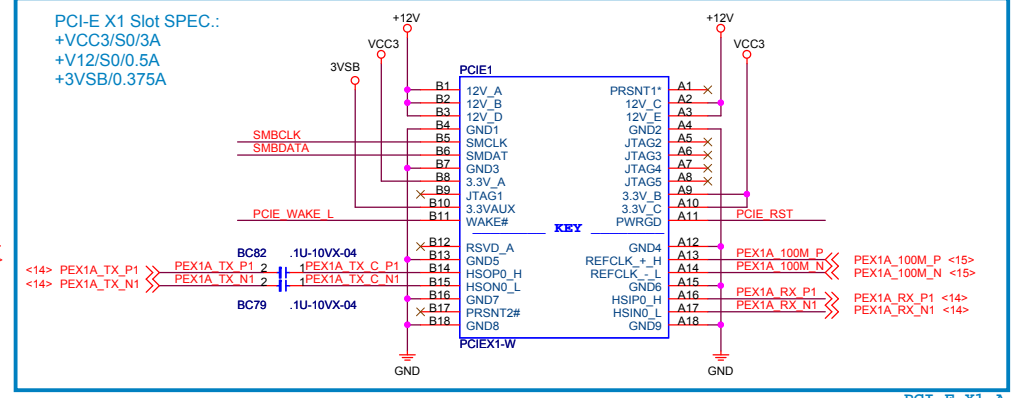
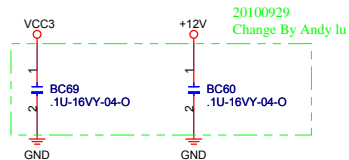
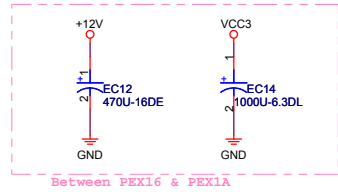
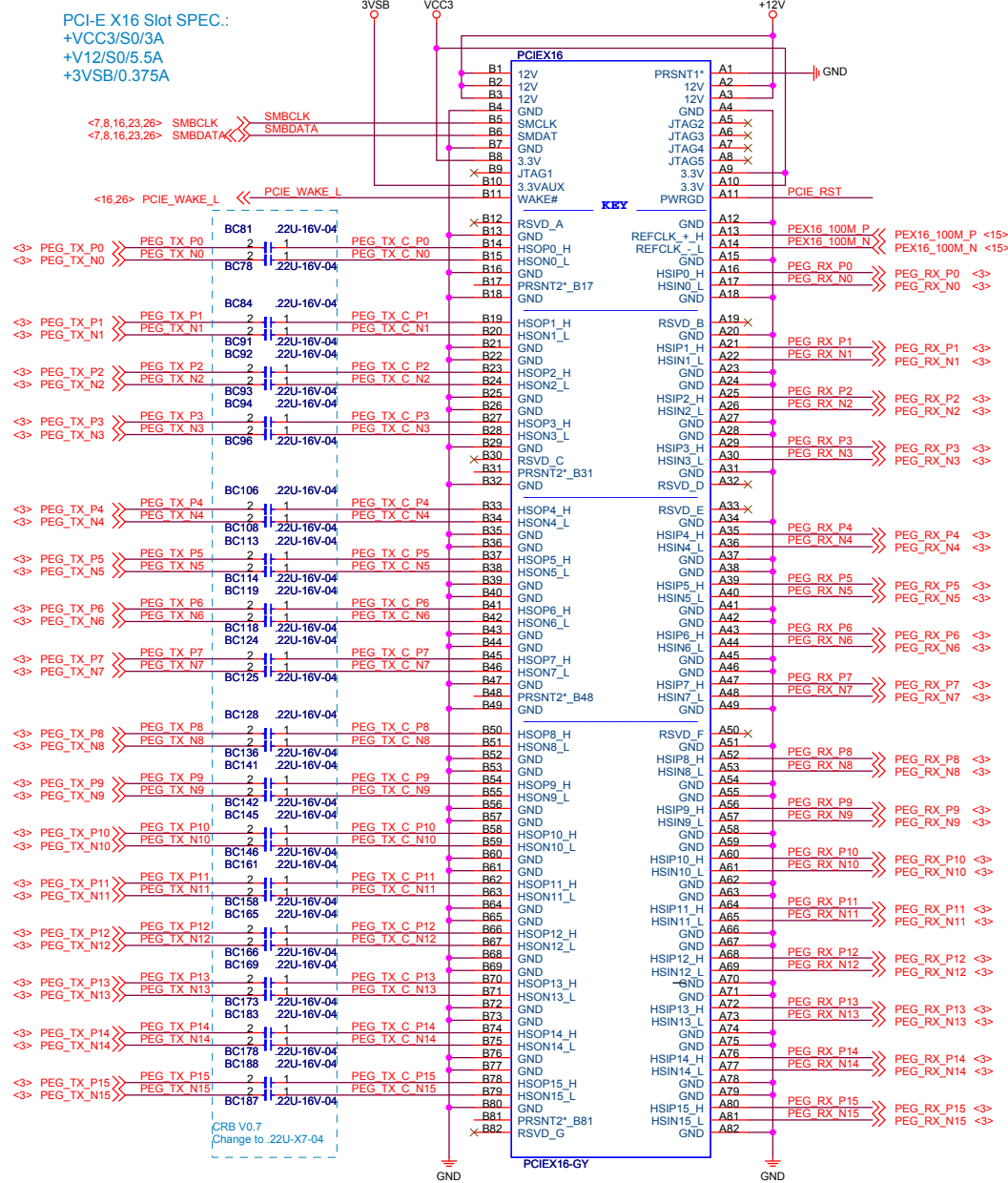
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Title		PCH - DMI/PCI/PE/USB	
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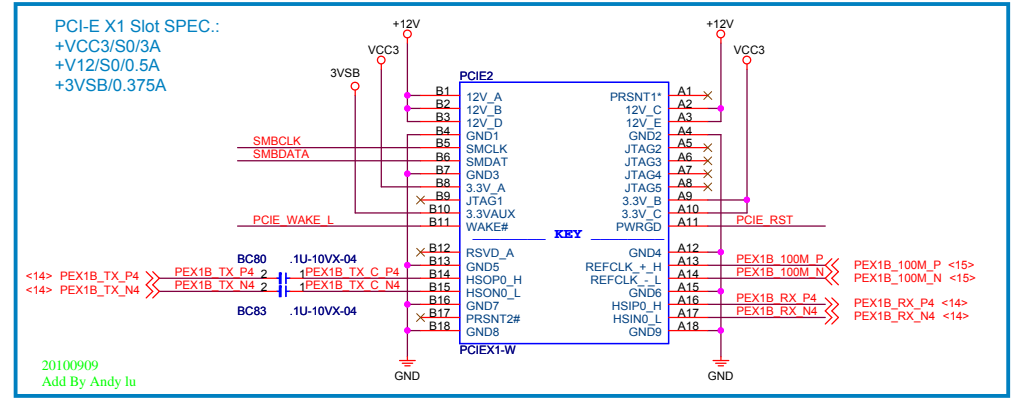
For H61:SATA port2/3 is disable....From 440377 file

**ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0,
ALSO SUPPORT SATA2.0, SATA1.0.**

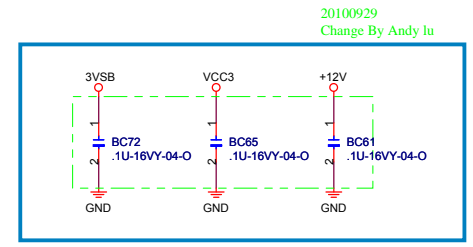




PCI-E X1 A

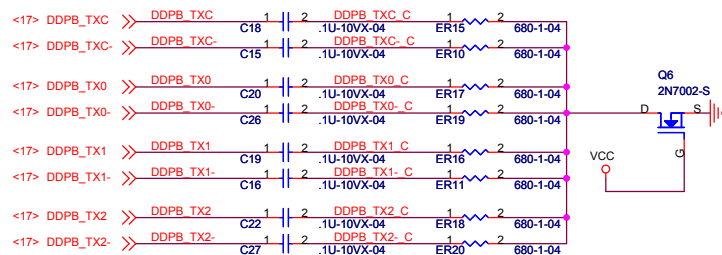


PCI-E X1 B

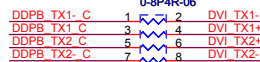
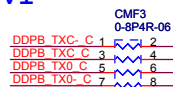


PCI-E X1 A Decoupling Cap.

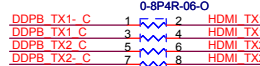
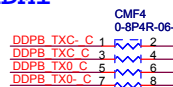
20100929
Change By Andy lu



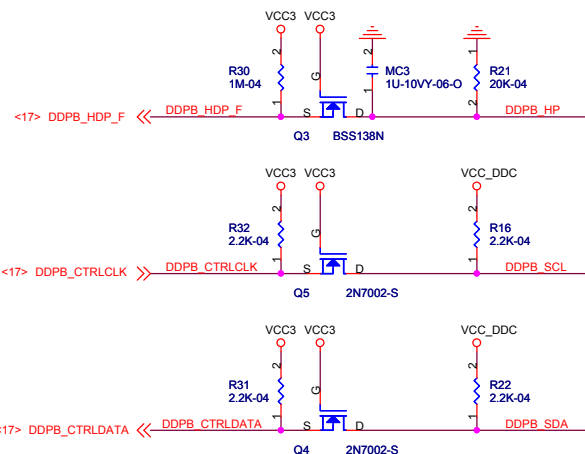
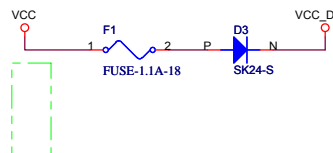
DVI



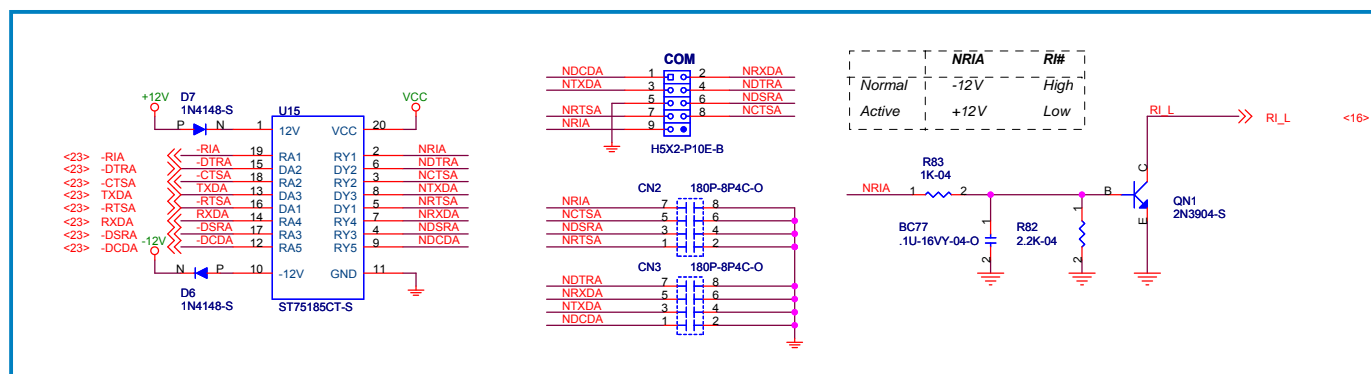
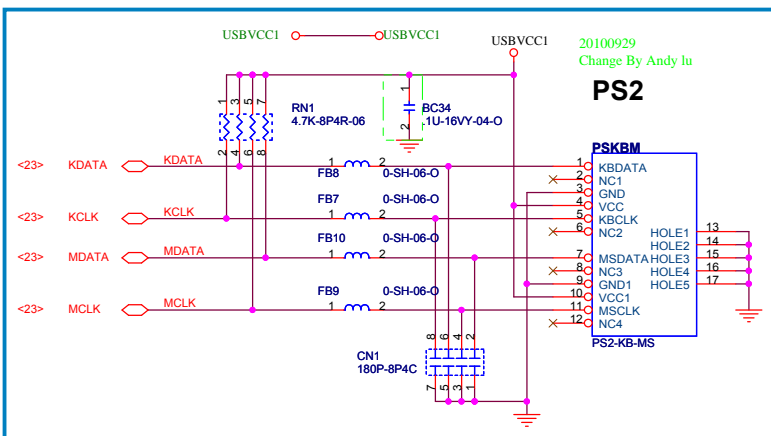
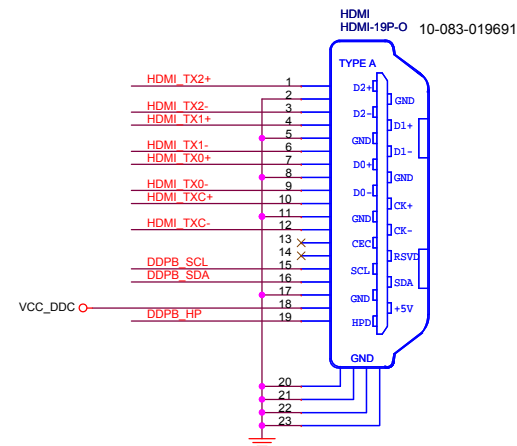
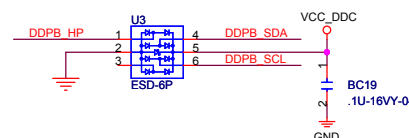
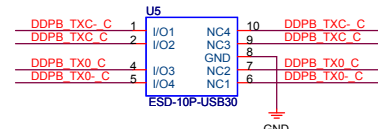
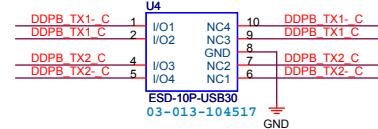
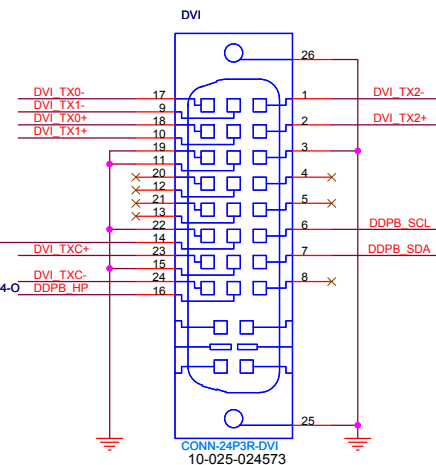
HDMI



20100928
 Del MC 10UF
 By Andy lu



20100929
 Change By Andy lu



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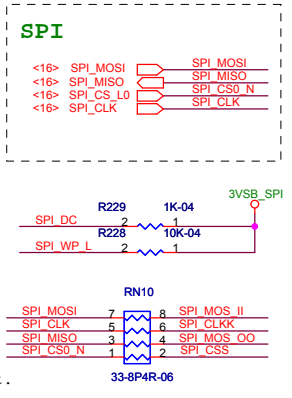
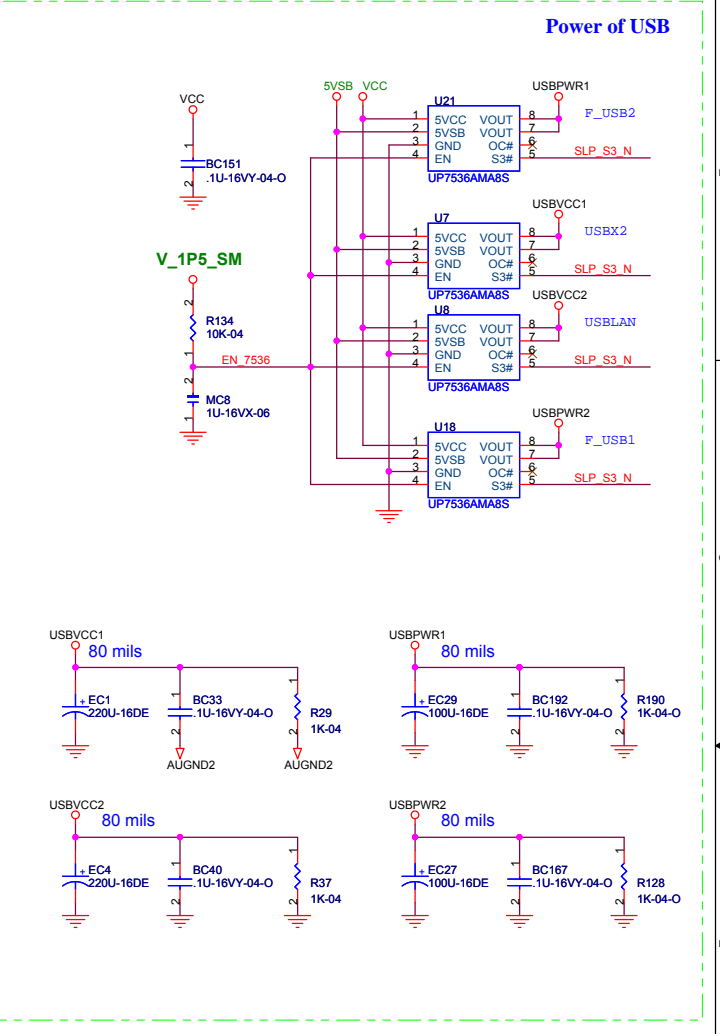
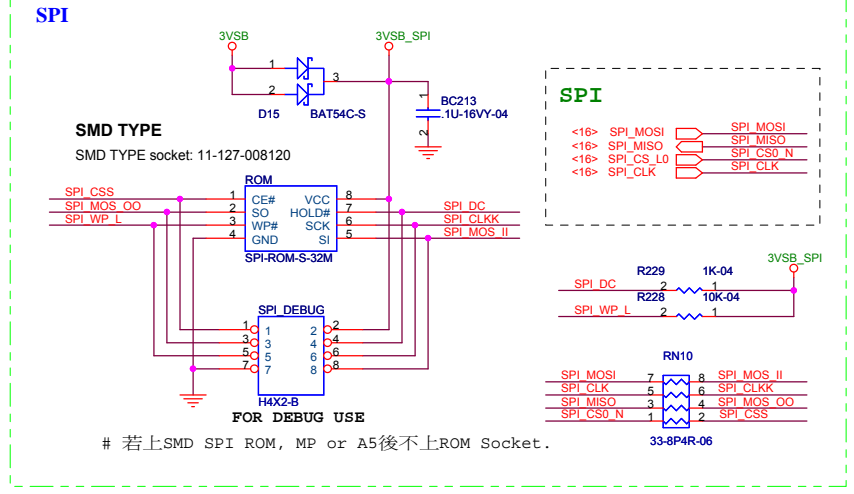
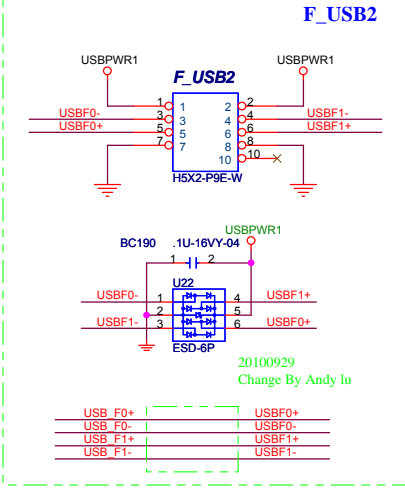
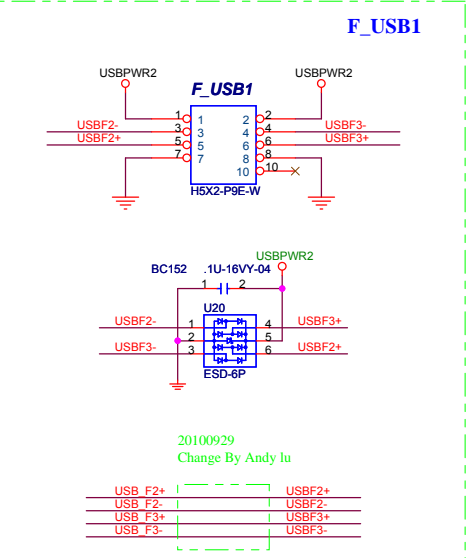
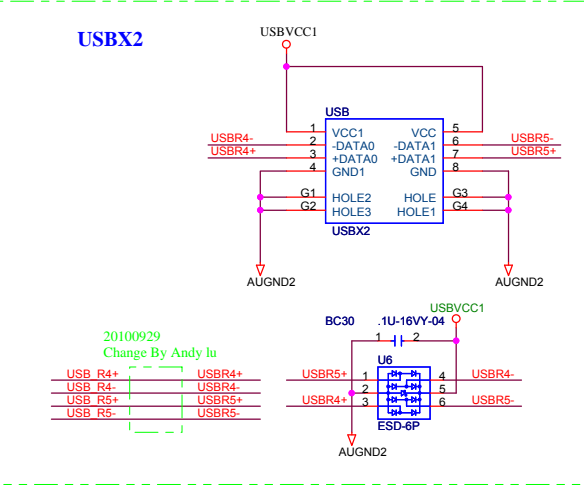
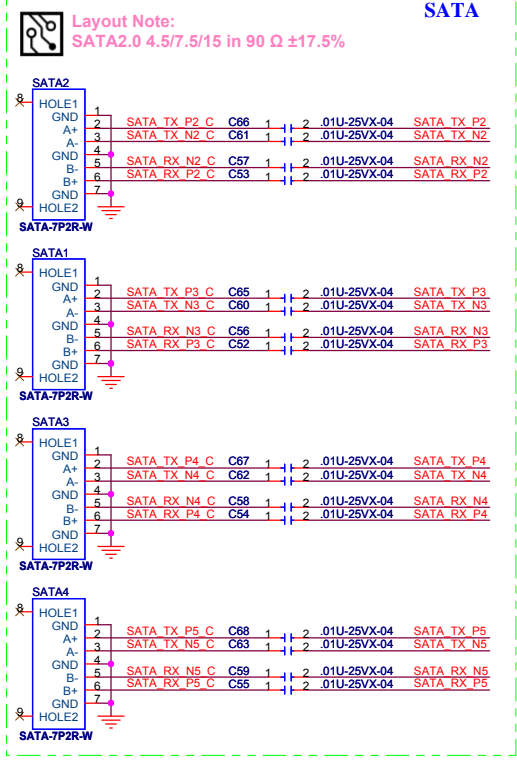
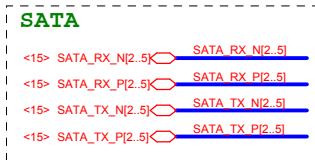
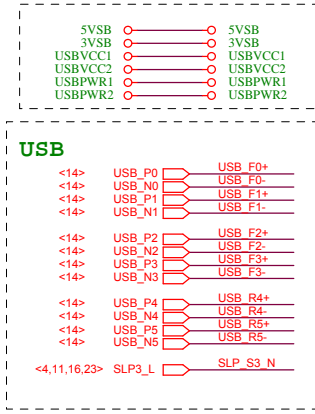
Title: **DVI&HDMI CONN&COM&PS2**

Size: **H61H2-M2**

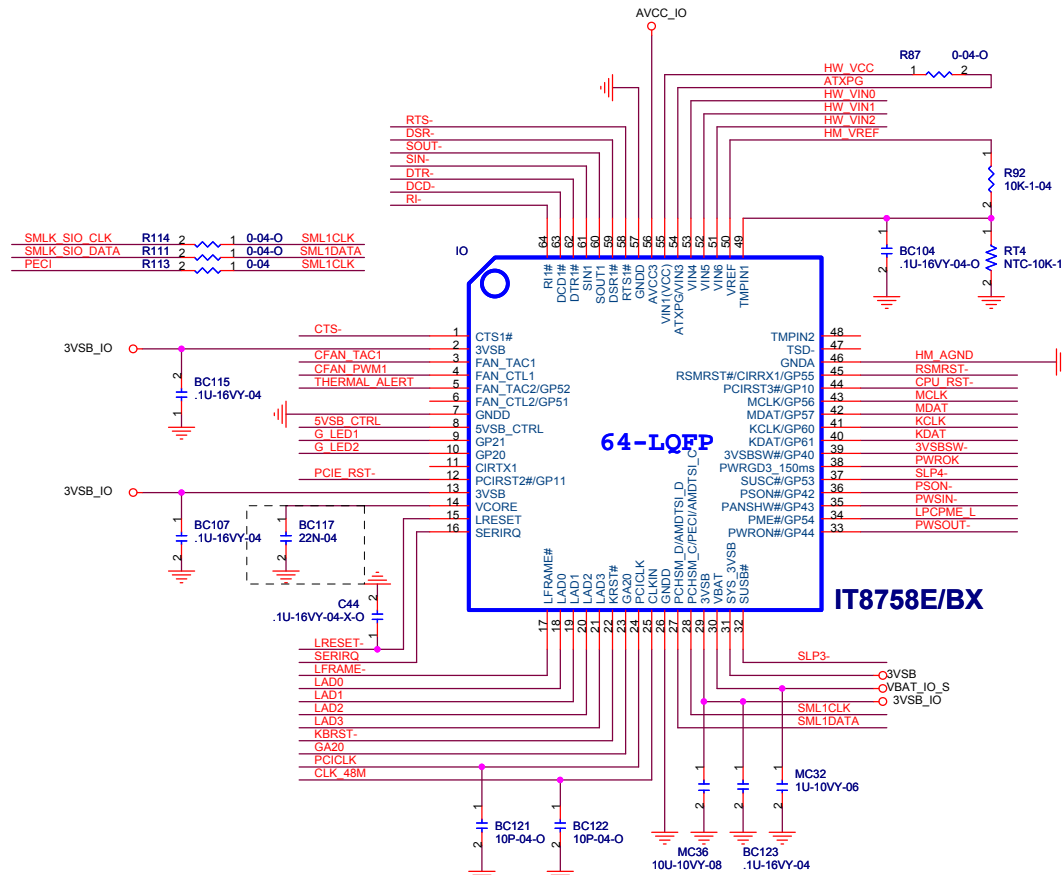
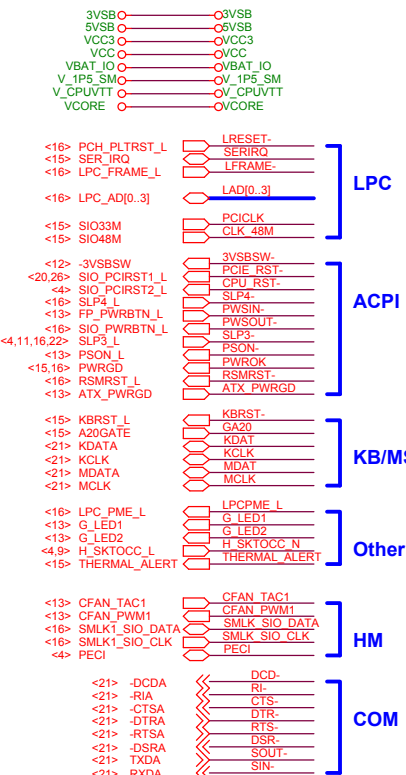
Custom: **Rev 1.0**

Date: **Tuesday, December 14, 2010**

Sheet: **21** of **29**

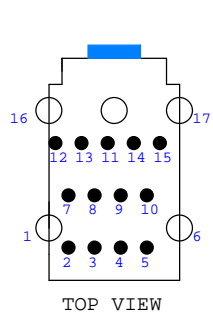
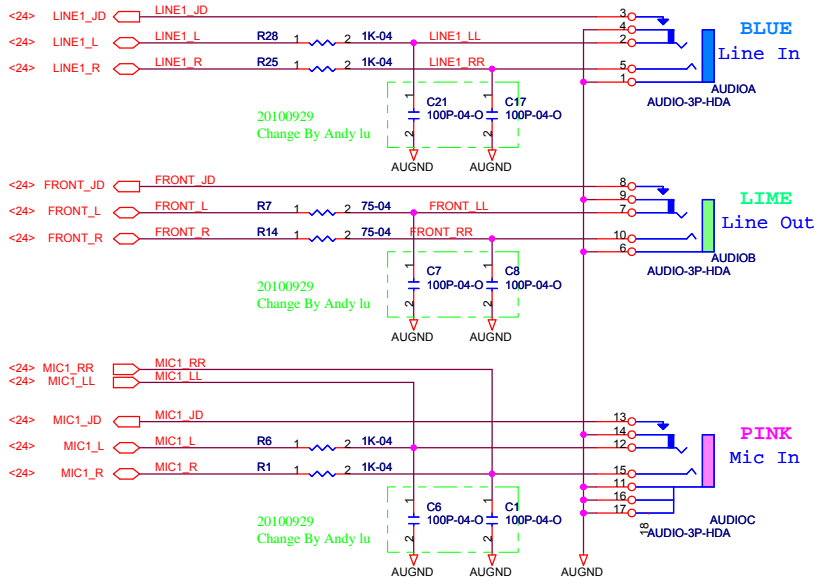


External Connection



<16> FP_AUD_DETECT << HDPANEL_DETECT

Non re-tasking for rear panel

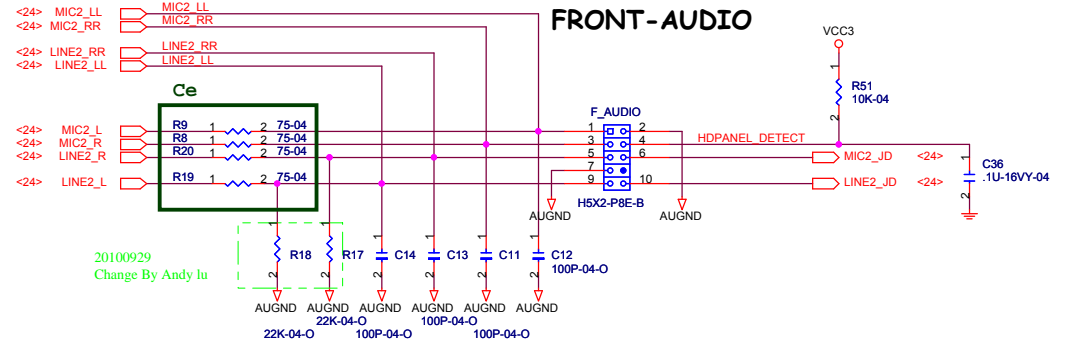


TOP VIEW

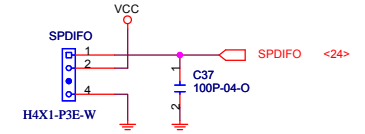


FRONT VIEW

FRONT-AUDIO



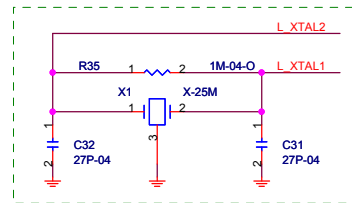
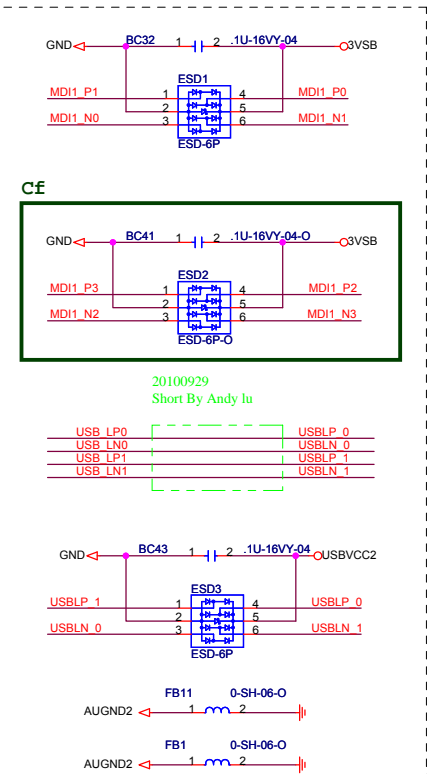
SPDIF-OUT



Connectivity diagram for the i.MX6Q processor. The diagram shows various pins on the left connected to internal blocks on the right.

- USBVCC2** (Pin) connects to **USBVCC2** (Block).
- 3VSB** (Pin) connects to **3VSB** (Block).
- VCC3** (Pin) connects to **VCC3** (Block).
- AUGND2** (Pin) connects to **AUGND2** (Block).
- PCIE_WAKE_L** (Pin) connects to **PCIE_LANE1_RST-** (Block).
- SIO_PCIE1ST_L** (Pin) connects to **CK_LANE1_H** (Block).
- CK_LANE100M_LAN_L** (Pin) connects to **CK_LANE1_L** (Block).
- LAN_TX_P6** (Pin) connects to **LAN1_HSIP** (Block).
- LAN_TX_N6** (Pin) connects to **LAN1_HSIN** (Block).
- LAN_RX_P6** (Pin) connects to **LAN1_HSOP** (Block).
- LAN_RX_N6** (Pin) connects to **LAN1_HSON** (Block).
- USB_N10** (Pin) connects to **USB_LN0** (Block).
- USB_P10** (Pin) connects to **USB_LP0** (Block).
- USB_N11** (Pin) connects to **USB_LN1** (Block).
- USB_P11** (Pin) connects to **USB_LP1** (Block).
- SMBCLK** (Pin) connects to **SMBCLK** (Block).
- SMBDATA** (Pin) connects to **SMBDATA** (Block).

LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap



	AR8151-B 1000M	AR8152-B 10/100M	AR8161-B 1000M
Ca	AR8151-B	AR8152-B	AR8161-B
Cb	V	X	X
Cc	USBX2-LAN-1000	USBX2-LAN-100	USBX2-LAN-1000
Cd	X	V	X
Ce	0-04	.01U-25VX-04	0-04
Cf	V	X	V
Cg	V	X	X
Ch	X	V	X
Ci	V	V	X
Cj	V	X	V
Ck	V	X	X
Cl	X	X	V
Cm	V	V	X
Cn	V	V	X

1 LAN_LED0 R42 1 2 330-04 ACTIVE_Y

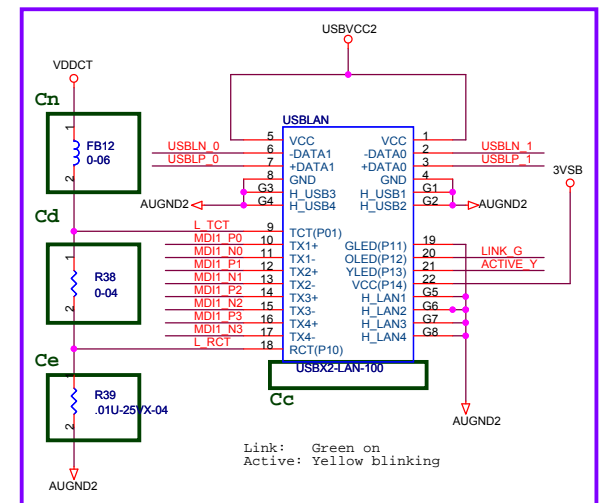
0 LAN_LED1 R40 1 2 330-04 LINK_G

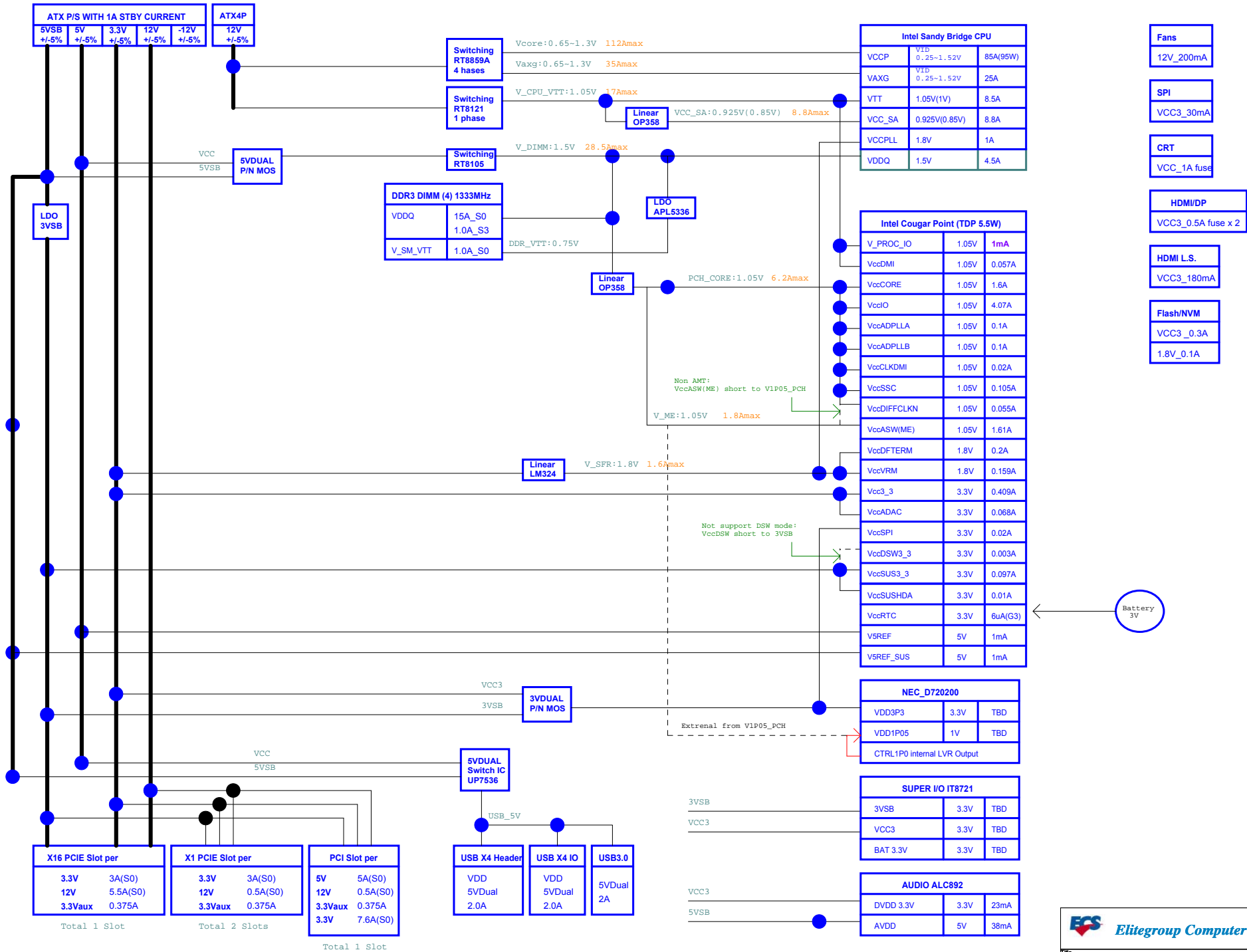
R41 1 2 5.1K-04

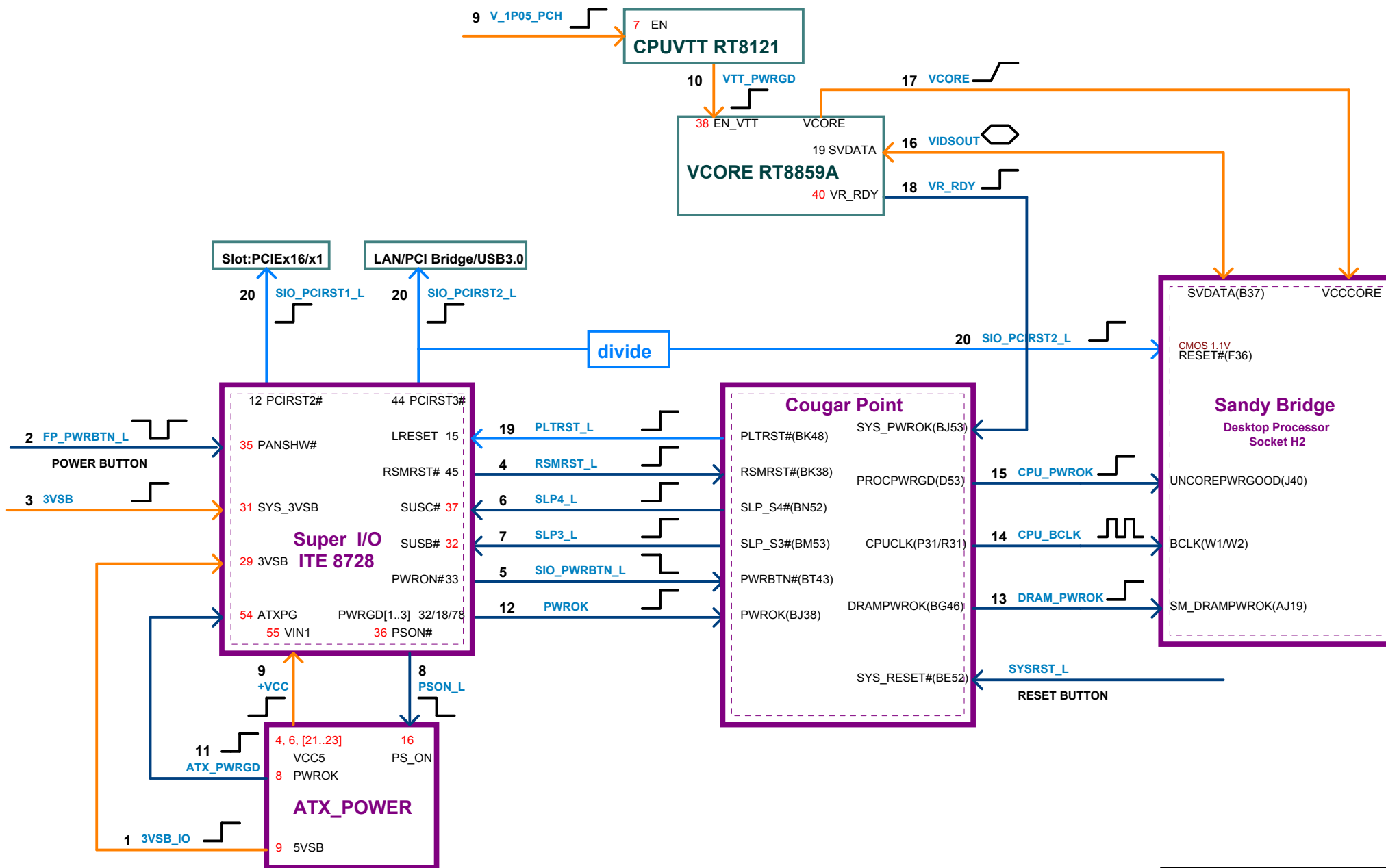
DVDDL	BC38	1	2	.1U-10VX-04	PIN24
AVDDL	BC36	1	2	.1U-10VX-04	PIN34
AVDDL	BC37	1	2	.1U-10VX-04	PIN31
AVDDH	BC20	1	2	.1U-10VX-04	PIN22
VDDCT	BC28	1	2	.1U-10VX-04	PIN5

AVDDL MC4 1 2 1U-10VY-06 PIN6

AVDDH MC1 1 2 1U-10VY-06 PIN9







NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

